VND5050AJ-E
VND5050AK-E

Double channel high side driver with analog current sense for automotive applications

Features

Max transient supply voltage	V_{CC}	41 V
Operating voltage range	V_{CC}	4.5 to 36 V
Max on-state resistance (per ch.)	R_{ON}	50 mΩ
Current limitation (typ)	I_{LIMH}	18 A
Off-state supply current	I_S	2 µA(1)

1. Typical value with all loads connected

- Main
  - Inrush current active management by power limitation
  - Very low standby current
  - 3.0 V CMOS compatible input
  - Optimized electromagnetic emission
  - Very low electromagnetic susceptibility
  - In compliance with the 2002/95/ec european directive
- Diagnostic functions
  - Proportional load current sense
  - High current sense precision for wide range currents
  - Current sense disable
  - Thermal shutdown indication
  - Very low current sense leakage
- Protections
  - Undervoltage shutdown
  - Overvoltage clamp
  - Load current limitation
  - Self limiting of fast thermal transients
  - Protection against loss of ground and loss of V_{CC}
  - Thermal shutdown
  - Reverse battery protection (see *Application schematic on page 21*)
  - Electrostatic discharge protection


PowerSSO-12


PowerSSO-24

Applications

- All types of resistive, inductive and capacitive loads
- Suitable as LED driver

Description

The VND5050AJ-E, VND5050AK-E is a monolithic device made using STMicroelectronics VIPower M0-5 technology. It is intended for driving resistive or inductive loads with one side connected to ground. Active V_{CC} pin voltage clamp protects the device against low energy spikes (see ISO7637 transient compatibility table).

This device integrates an analog current sense which delivers a current proportional to the load current (according to a known ratio) when CS_DIS is driven low or left open. When CS_DIS is driven high, the current sense pin is in a high impedance condition.

Output current limitation protects the device in overload condition. In case of long overload duration, the device limits the dissipated power to safe level up to thermal shutdown intervention. Thermal shutdown with automatic restart allows the device to recover normal operation as soon as fault condition disappears.

Table 1. Device summary

Package	Order codes	
	Tube	Tape and reel
PowerSSO-12	VND5050AJ-E	VND5050AJTR-E
PowerSSO-24	VND5050AK-E	VND5050AKTR-E

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1 Block diagram and pin description

Figure 1. Block diagram

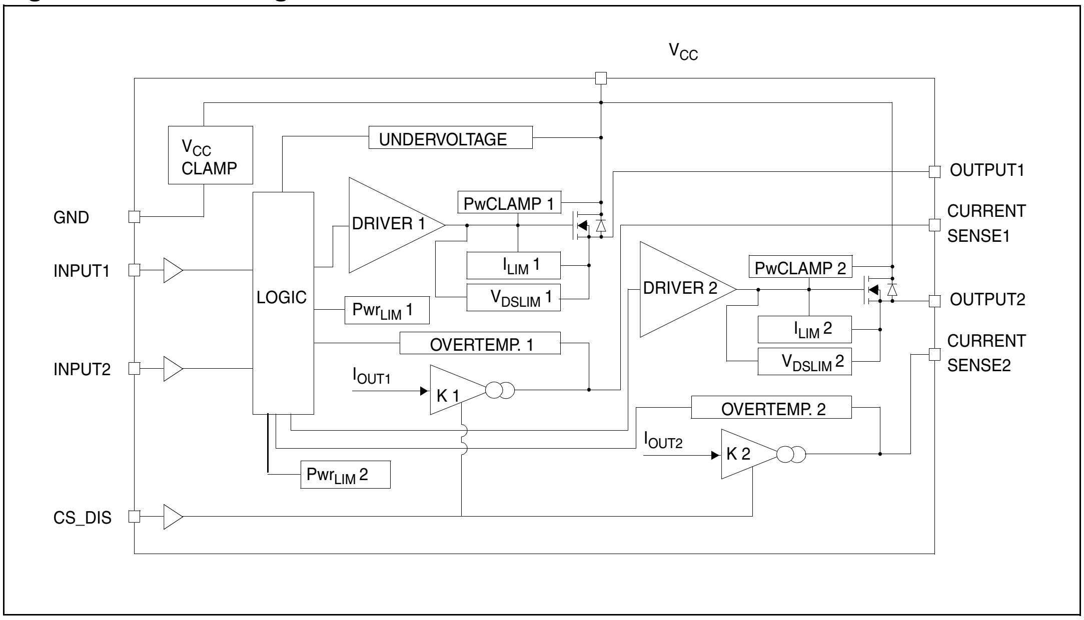


Table 2. Pin function

Name	Function
V_{CC}	Battery connection.
$OUTPUT_{1,2}$	Power output.
GND	Ground connection. Must be reverse battery protected by an external diode/resistor network.
$INPUT_{1,2}$	Voltage controlled input pin with hysteresis, CMOS compatible. Controls output switch state.
CURRENT $SENSE_{1,2}$	Analog current sense pin, delivers a current proportional to the load current
CS_DIS	Active high CMOS compatible pin, to disable the current sense pin.

Figure 2. Configuration diagram (top view)

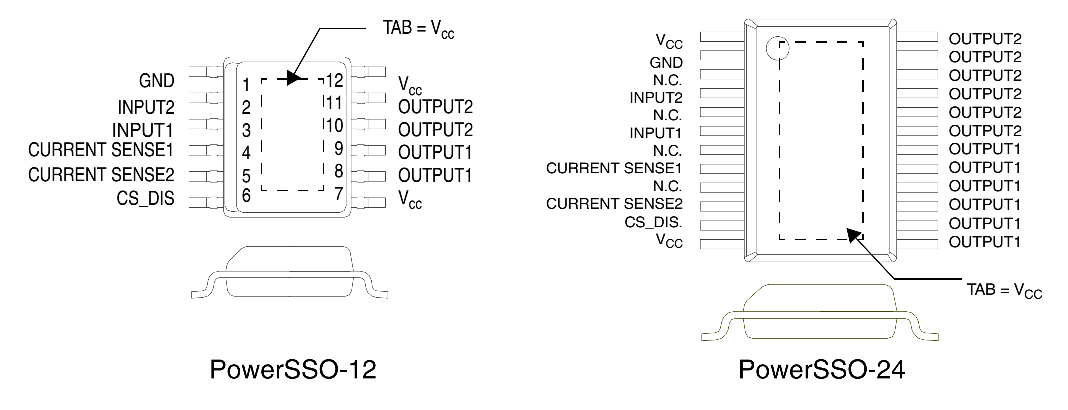


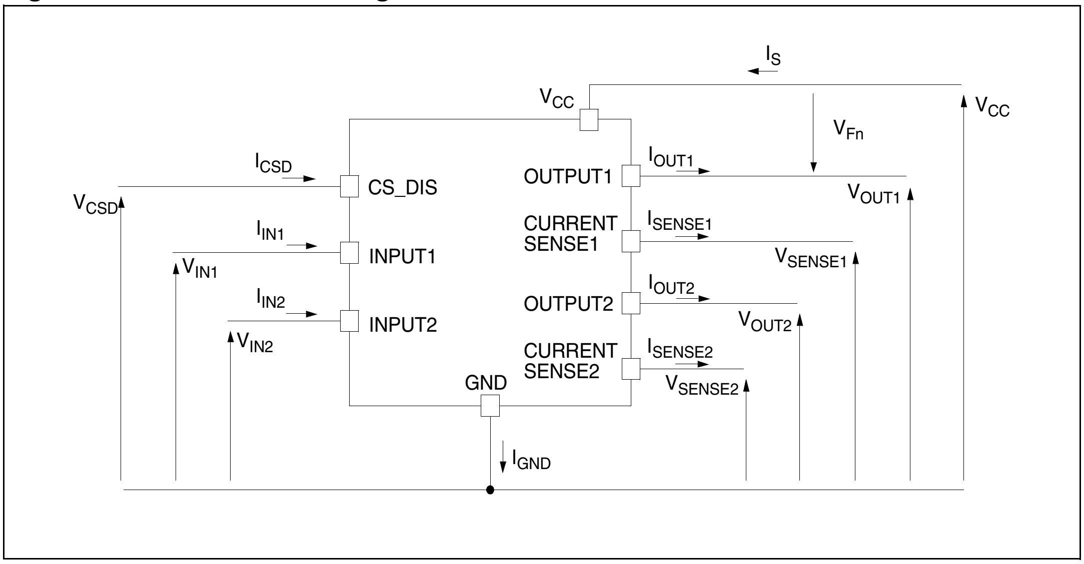
Table 3. Suggested connections for unused and not connected pins

Connection/pin	Current sense	N.C.	Output	Input	CS_DIS
Floating	N.R.(1)	X	X	X	X
To ground	Through 1 KΩ resistor	X	N.R.(1)	Through 10 KΩ resistor	Through 10 KΩ resistor

1. Not recommended.

2 Electrical specifications

Figure 3. Current and voltage conventions



Note: $V_{Fn} = V_{OUTn} - V_{CC}$ during reverse battery condition.

2.1 Absolute maximum ratings

Stressing the device above the rating listed in the “Absolute maximum ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to the conditions in table below for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality document.

Table 4. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	DC supply voltage	41	V
$-V_{CC}$	Reverse DC supply voltage	0.3	V
$-I_{GND}$	DC reverse ground pin current	200	mA
I_{OUT}	DC output current	Internally limited	A
$-I_{OUT}$	Reverse DC output current	12	A
I_{IN}	DC input current	-1 to 10	mA
I_{CSD}	DC current sense disable input current	-1 to 10	mA
$-I_{CSENSE}$	DC reverse CS pin current	200	mA
V_{CSENSE}	Current sense maximum voltage	V_{CC}-41 +V_{CC}	V V
E_{MAX}	Maximum switching energy (L= 3mH; R_L=0Ω; V_{bat}=13.5V; T_{jstart}=150°C; I_{OUT} = I_{limL}*(Typ.)*)	104	mJ

Table 4. Absolute maximum ratings (continued)

Symbol	Parameter	Value	Unit
V_{ESD}	Electrostatic discharge (Human Body Model: R=1.5KΩ; C=100pF) – Input – Current sense – CS_DIS – Output – V_{CC}	 4000 2000 4000 5000 5000	 V V V V V
V_{ESD}	Charge device model (CDM-AEC-Q100-011)	750	V
T_j	Junction operating temperature	-40 to 150	°C
T_{stg}	Storage temperature	-55 to 150	°C

2.2 Thermal data

Table 5. Thermal data

Symbol	Parameter	Value		Unit
		PowerSSO-12	PowerSSO-24	
$R_{thj-case}$	Thermal resistance junction case (max) (with one channel on)	2.7	2.7	°C/W
$R_{thj-amb}$	Thermal resistance junction ambient (max)	See *Figure 29*	See *Figure 33*	°C/W

2.3 Electrical characteristics

8 V<V_{CC}<36 V; -40 °C<T_j<150 °C, unless otherwise specified.

Table 6. Power section

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{CC}	Operating supply voltage		4.5	13	36	V
V_{USD}	Undervoltage shutdown			3.5	4.5	V
$V_{USDhyst}$	Undervoltage shutdown hysteresis			0.5		V
R_{ON}	On-state resistance(1)	I_{OUT}= 2A; T_j= 25°C I_{OUT}= 2A; T_j= 150°C I_{OUT}= 2A; V_{CC}= 5V; T_j= 25°C			50 100 65	mΩ mΩ mΩ
V_{clamp}	Clamp voltage	I_S= 20mA	41	46	52	V
I_S	Supply current	Off-state; V_{CC}=13V; T_j=25°C; V_{IN}=V_{OUT}=V_{SENSE}=V_{CSD}=0V On-state; V_{CC}=13V; V_{IN}=5V; I_{OUT}= 0A		2(2) 3	5(2) 6	µA mA

Table 6. Power section (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{L(off)}$	Off-state output current(1)	$V_{IN}=V_{OUT}=0V$; $V_{CC}=13V$; $T_j= 25°C$ $V_{IN}=V_{OUT}=0V$; $V_{CC}=13V$; $T_j= 125°C$	0 0	0.01	3 5	µA
V_F	Output - V_{CC} diode voltage (1)	$-I_{OUT}=4A$; $T_j=150°C$			0.7	V

1. For each channel.
2. PowerMOS leakage included.

Table 7. Switching (V_{CC} = 13V; T_j = 25°C)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	R_L= 6.5Ω (see *Figure 8*)		25		µs
$t_{d(off)}$	Turn-off delay time	R_L= 6.5Ω (see *Figure 8*)		35		µs
$dV_{OUT}/dt_{(on)}$	Turn-on voltage slope	R_L= 6.5Ω	See *Figure 21*			V/µs
$dV_{OUT}/dt_{(off)}$	Turn-off voltage slope	R_L= 6.5Ω	See *Figure 22*			V/µs
W_{ON}	Switching energy losses during t_{won}	R_L= 6.5Ω (see *Figure 8*)		0.24		mJ
W_{OFF}	Switching energy losses during t_{woff}	R_L= 6.5Ω (see *Figure 8*)		0.2		mJ

Table 8. Logic input

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IL}	Input low level voltage				0.9	V
I_{IL}	Low level input current	V_{IN}= 0.9V	1			µA
V_{IH}	Input high level voltage		2.1			V
I_{IH}	High level input current	V_{IN}= 2.1V			10	µA
$V_{I(hyst)}$	Input hysteresis voltage		0.25			V
V_{ICL}	Input clamp voltage	I_{IN}= 1mA I_{IN}= -1mA	5.5	 -0.7	7	V V
V_{CSDL}	CS_DIS low level voltage				0.9	V
I_{CSDL}	Low level CS_DIS current	V_{CSD}= 0.9V	1			µA
V_{CSDH}	CS_DIS high level voltage		2.1			V
I_{CSDH}	High level CS_DIS current	V_{CSD}= 2.1V			10	µA

Table 8. Logic input (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{CSD(hyst)}$	CS_DIS hysteresis voltage		0.25			V
V_{CSCL}	CS_DIS clamp voltage	I_{CSD}= 1mA I_{CSD}= -1mA	5.5	 -0.7	7	V V

Table 9. Protections and diagnostics [(1)]

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{limH}	DC short circuit current	V_{CC}= 13V 5V<V_{CC}<36V	12	18	24 24	A A
I_{limL}	Short circuit current during thermal cycling	V_{CC}=13V; T_R<T_j<T_{TSD}		7		A
T_{TSD}	Shutdown temperature		150	175	200	°C
T_R	Reset temperature		T_{RS} + 1	T_{RS} + 5		°C
T_{RS}	Thermal reset of STATUS		135			°C
T_{HYST}	Thermal hysteresis (T_{TSD}-T_R)			7		°C
V_{DEMAG}	Turn-off output voltage clamp	I_{OUT}=2A; V_{IN}=0; L=6mH	V_{CC}-41	V_{CC}-46	V_{CC}-52	V
V_{ON}	Output voltage drop limitation	I_{OUT}=0.1A; T_j= -40°C...+150°C (see *Figure 9*)		25		mV

1. To ensure long term reliability under heavy overload or short circuit conditions, protection and related diagnostic signals must be used together with a proper software strategy. If the device is subjected to abnormal conditions, this software must limit the duration and number of activation cycles.

Table 10. Current sense (8V<V_{CC}<16V)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
K_0	I_{OUT}/I_{SENSE}	I_{OUT}=0.05A; V_{SENSE}=0.5V;V_{CSD}=0V; T_j= -40°C...150°C	1270	2360	3450	
K_1	I_{OUT}/I_{SENSE}	I_{OUT}=1A; V_{SENSE}=0.5V;V_{CSD}=0V; T_j= -40°C T_j= 25°C...150°C	1470 1570	2020 2020	2610 2470	
dK_1/K_1[(1)]	Current sense ratio drift	I_{OUT}=1A; V_{SENSE}= 0.5V; V_{CSD}=0V; T_J=-40 °C to 150 °C	-7		+7	%
K_2	I_{OUT}/I_{SENSE}	I_{OUT}=2A; V_{SENSE}=4V;V_{CSD}=0V; T_j= -40°C T_j= 25°C...150°C	1740 1790	2020 2020	2320 2250	

Table 10. Current sense (8V<V_{CC}<16V) (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
dK_2/K_2 (1)	Current sense ratio drift	I_{OUT}=2 A; V_{SENSE}= 4 V; V_{CSD}=0V; T_J=-40 °C to 150 °C	-4		+4	%
K_3	I_{OUT}/I_{SENSE}	I_{OUT}=4A; V_{SENSE}=4V;V_{CSD}=0V; T_j=-40°C T_j=25°C...150°C	1880 1900	2010 2010	2160 2120	
dK_3/K_3 (1)	Current sense ratio drift	I_{OUT}=4 A; V_{SENSE}= 4 V; V_{CSD}=0V; T_J=-40 °C to 150 °C	-2		+2	%
I_{SENSE0}	Analog sense leakage current	I_{OUT}=0A; V_{SENSE}=0V; V_{CSD}=5V; V_{IN}=0V; T_j=-40°C...150°C V_{CSD}=0V; V_{IN}=5V; T_j=-40°C...150°C I_{OUT}=2A; V_{SENSE}=0V; V_{CSD}=5V; V_{IN}=5V; T_j=-40°C...150°C	0 0 0		1 2 1	µA µA µA
I_{OL}	Openload on-state current detection threshold	V_{IN} = 5V, I_{SENSE}= 5 µA	4		20	mA
V_{SENSE}	Max analog sense output voltage	I_{OUT}=4A; V_{CSD}=0V	5			V
V_{SENSEH}	Analog sense output voltage in over temperature condition	V_{CC}=13V; R_{SENSE}=10KΩ		9		V
I_{SENSEH}	Analog sense output current in over temperature condition	V_{CC}=13V; V_{SENSE}=5V		8		mA
$t_{DSENSE1H}$	Delay response time from falling edge of CS_DIS pin	V_{SENSE}<4V, 0.5A<Iout<4A I_{SENSE}=90% of $I_{SENSE\ max}$ (see *Figure 4*)		50	100	µs
$t_{DSENSE1L}$	Delay response time from rising edge of CS_DIS pin	V_{SENSE}<4V, 0.5A<Iout<4A I_{SENSE}=10% of $I_{SENSE\ max}$ (see *Figure 4*)		5	20	µs
$t_{DSENSE2H}$	Delay response time from rising edge of INPUT pin	V_{SENSE}<4V, 0.5A<Iout<4A I_{SENSE}=90% of $I_{SENSE\ max}$ (see *Figure 4*)		80	250	µs

Table 10. Current sense (8V<V_{CC}<16V) (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$\Delta t_{DSENSE2H}$	Delay response time between rising edge of output current and rising edge of current sense	V_{SENSE} < 4V, I_{SENSE} = 90% of $I_{SENSEMAX}$, I_{OUT} = 90% of I_{OUTMAX} I_{OUTMAX}=2A (see *Figure 5*)			65	µs
$t_{DSENSE2L}$	Delay response time from falling edge of INPUT pin	V_{SENSE}<4V, 0.5A<Iout<4A I_{SENSE}=10% of $I_{SENSE\ max}$ (see *Figure 4*)		100	250	µs

1. Parameter guaranteed by design; it is not tested.

Figure 4. Current sense delay characteristics

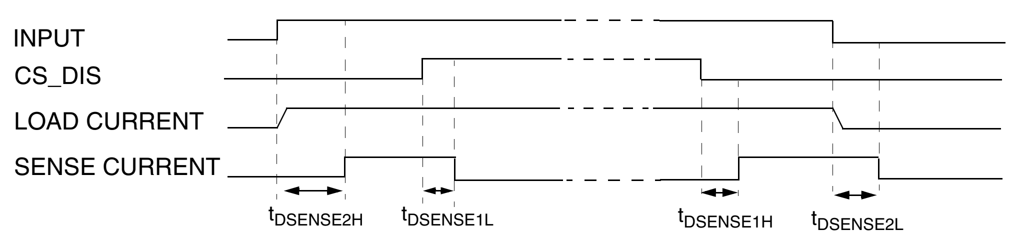


Figure 5. Delay response time between rising edge of output current and rising edge of current sense (CS enabled)

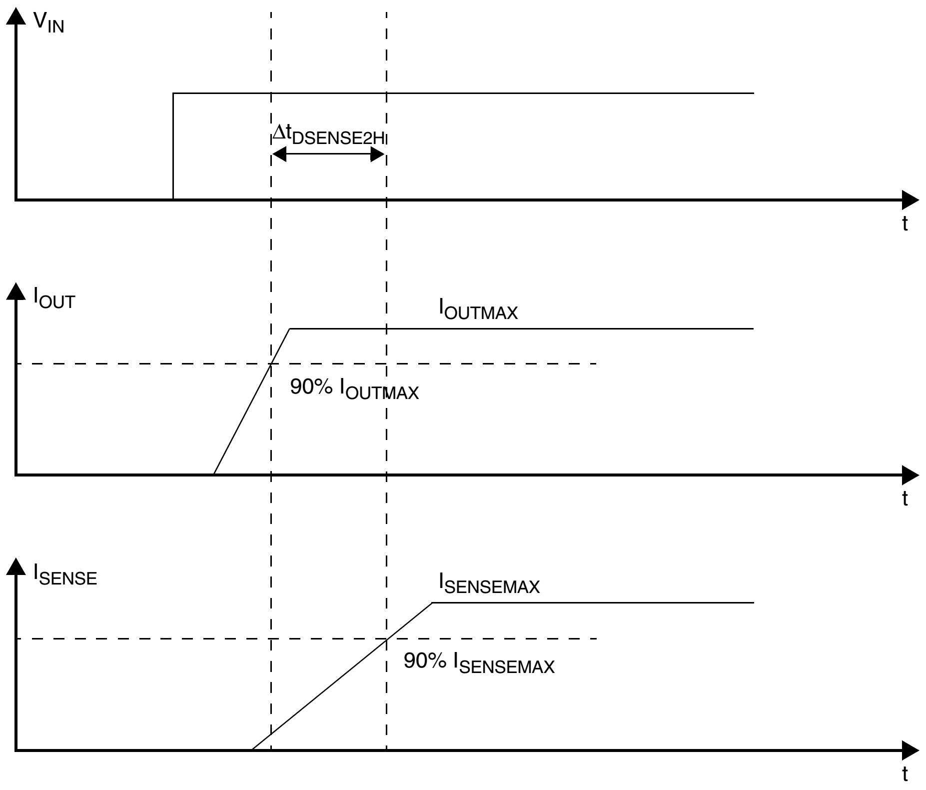


Figure 6. I_{OUT}/I_{SENSE} vs I_{OUT}

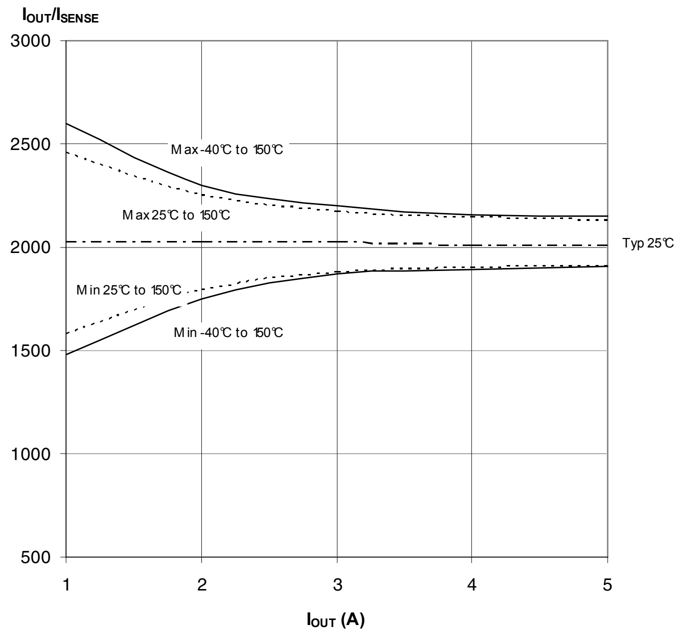
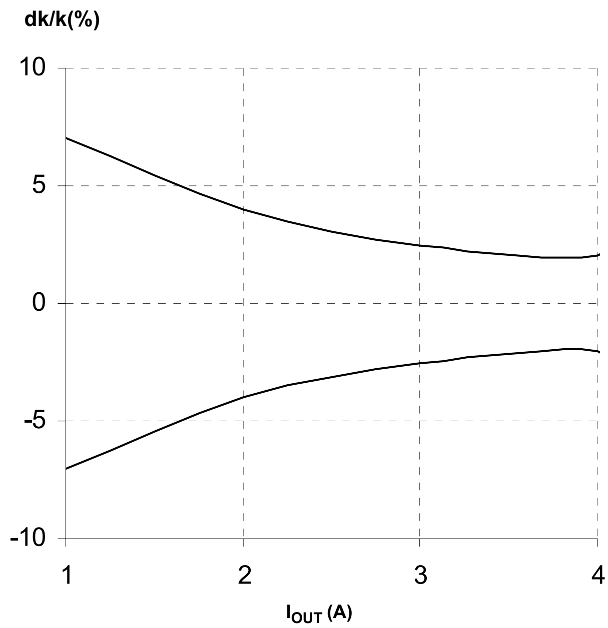


Figure 7. Maximum current sense ratio drift vs load current



Note: Parameter guaranteed by design; it is not tested.

Table 11. Truth table

Conditions	Input	Output	Sense (V_{CSD}=0V)[(1)]
Normal operation	L H	L H	0 Nominal
Over temperature	L H	L L	0 V_{SENSEH}
Undervoltage	L H	L L	0 0
Short circuit to GND ($R_{sc} \leq 10$ mΩ)	L H H	L L L	0 0 if $T_j < T_{TSD}$ V_{SENSEH} if $T_j > T_{TSD}$
Short circuit to V_{CC}	L H	H H	0 < Nominal
Negative output voltage clamp	L	L	0

1. If the V_{CSD} is high, the SENSE output is at a high impedance, its potential depends on leakage currents and external circuit.

Figure 8. Switching characteristics

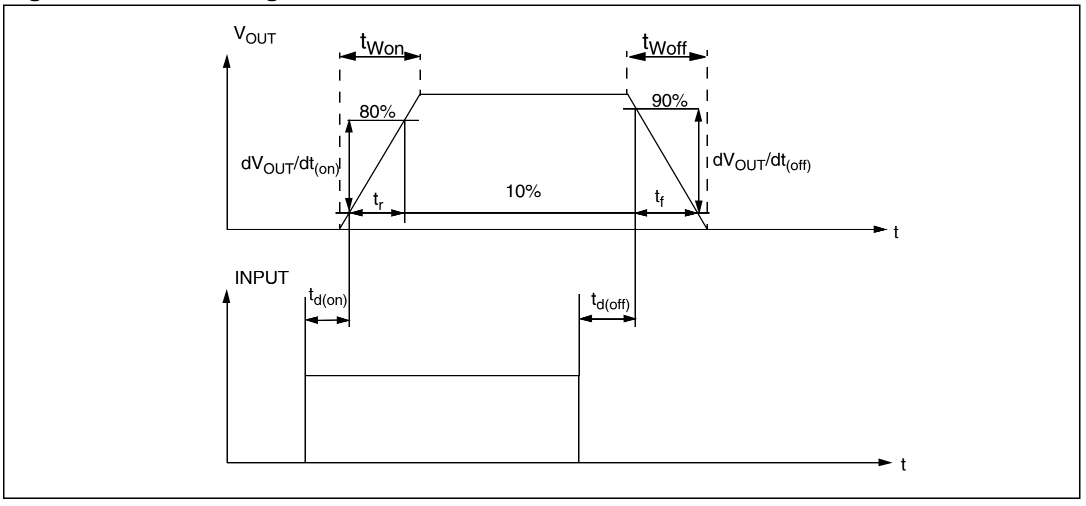


Figure 9. Output voltage drop limitation

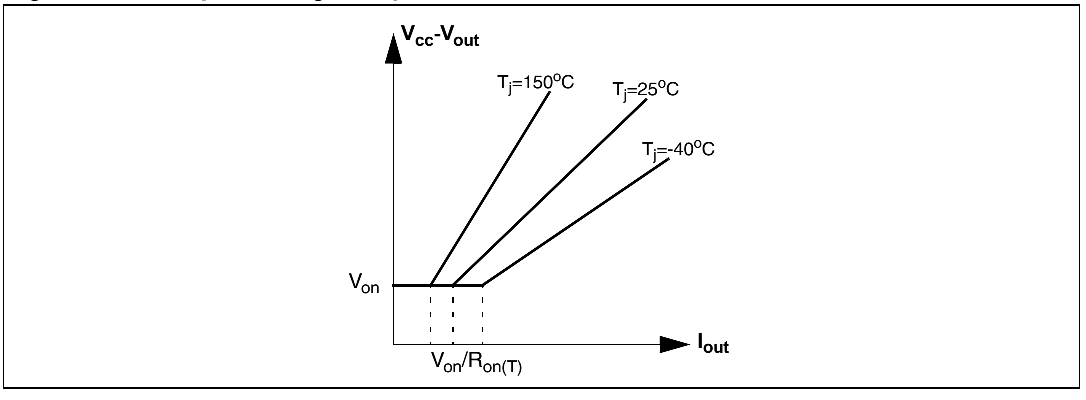


Table 12. Electrical transient requirements (part 1/3)

ISO 7637-2: 2004(E) test pulse	Test levels[1]		Number of pulses or test times	Burst cycle/pulse repetition time		Delays and impedance
	III	IV				
1	-75V	-100V	5000 pulses	0.5 s	5 s	2 ms, 10 Ω
2a	+37V	+50V	5000 pulses	0.2 s	5 s	50 µs, 2 Ω
3a	-100V	-150V	1h	90 ms	100 ms	0.1 µs, 50 Ω
3b	+75V	+100V	1h	90 ms	100 ms	0.1 µs, 50 Ω
4	-6V	-7V	1 pulse			100 ms, 0.01 Ω
5b [2]	+65V	+87V	1 pulse			400 ms, 2 Ω

1. The above test levels must be considered referred to V_{CC} = 13.5V except for pulse 5b.

Table 13. Electrical transient requirements (part 2/3)

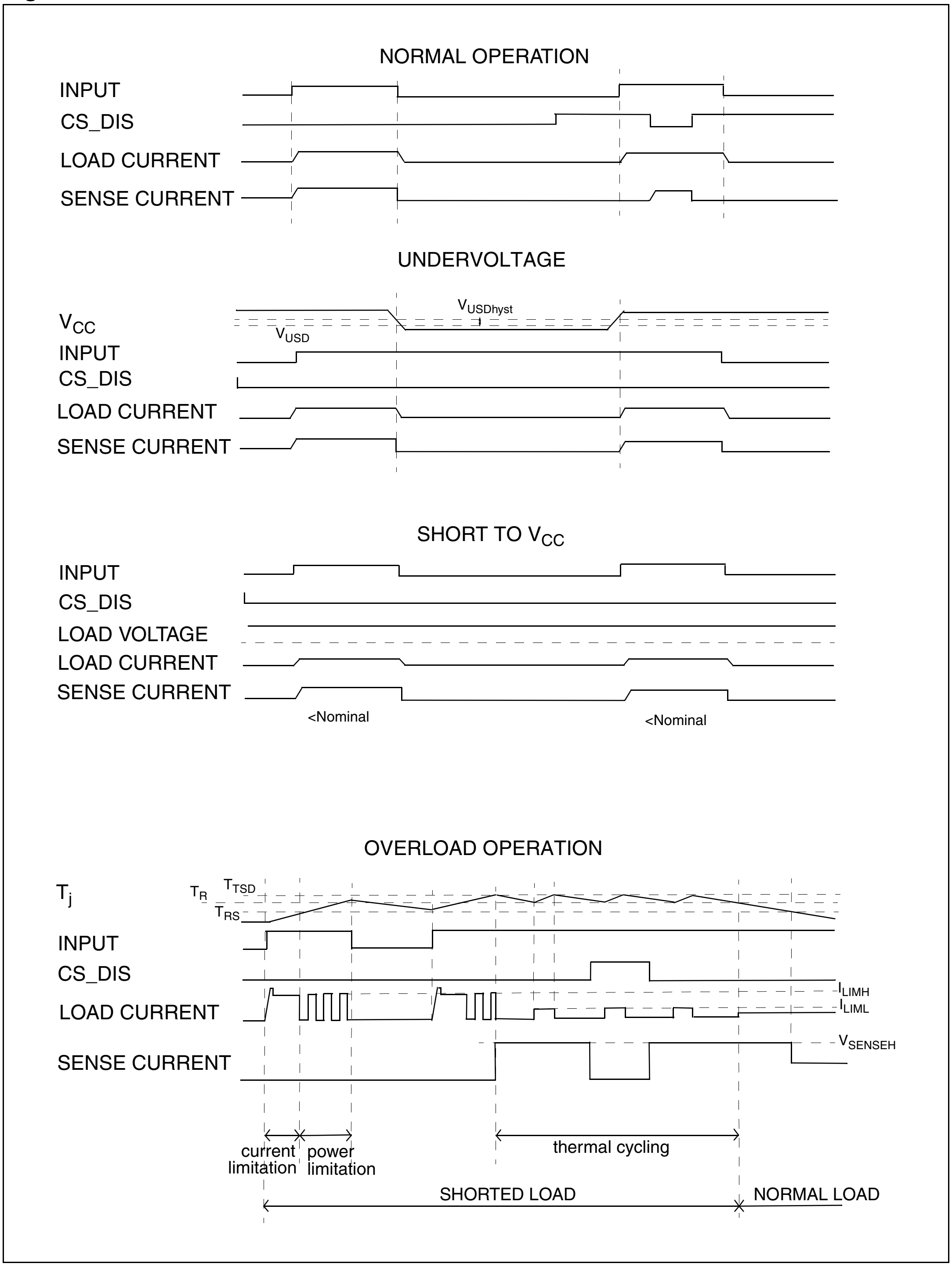
ISO 7637-2: 2004(E) test pulse	Test level results[1]	
	III	IV
1	C	C
2a	C	C
3a	C	C
3b	C	C
4	C	C
5b[2]	C	C

1. The above test levels must be considered referred to V_{CC} = 13.5V except for pulse 5b.
2. Valid in case of external load dump clamp: 40V maximum referred to ground.

Table 14. Electrical transient requirements (part 3/3)

Class	Contents
C	All functions of the device are performed as designed after exposure to disturbance.
E	One or more functions of the device are not performed as designed after exposure to disturbance and cannot be returned to proper operation without replacing the device.

Figure 10. Waveforms



2.4 Electrical characteristics curves

Figure 11. Off-state output current

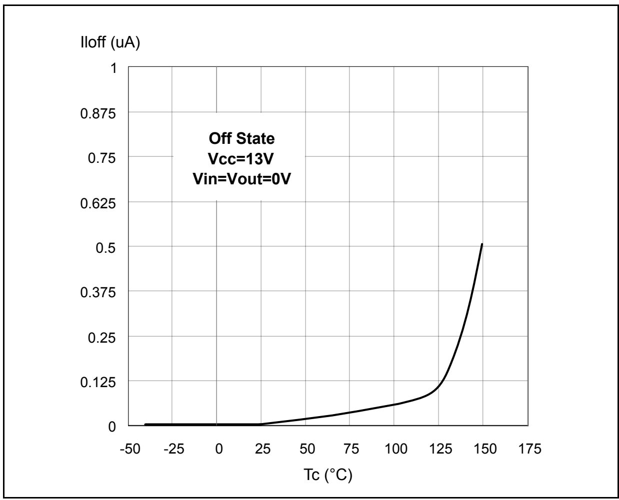


Figure 12. High level input current

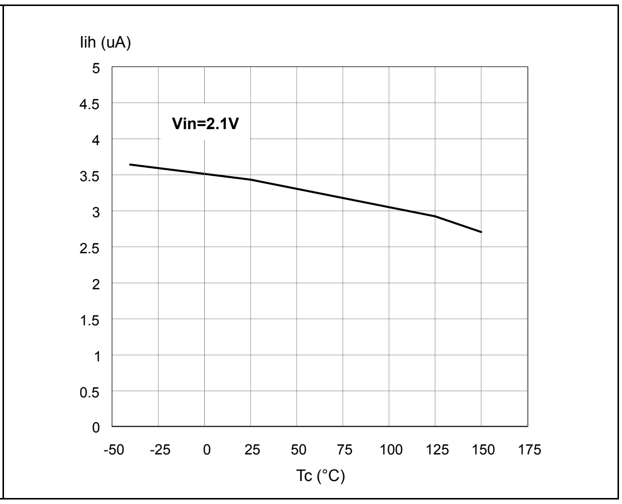


Figure 13. Input clamp voltage

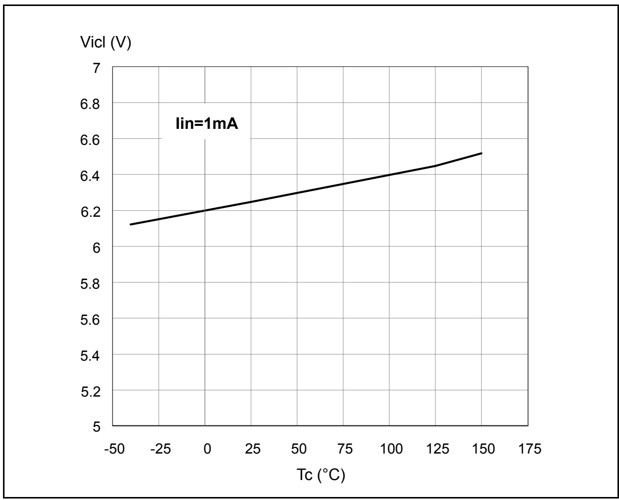


Figure 14. Input high level

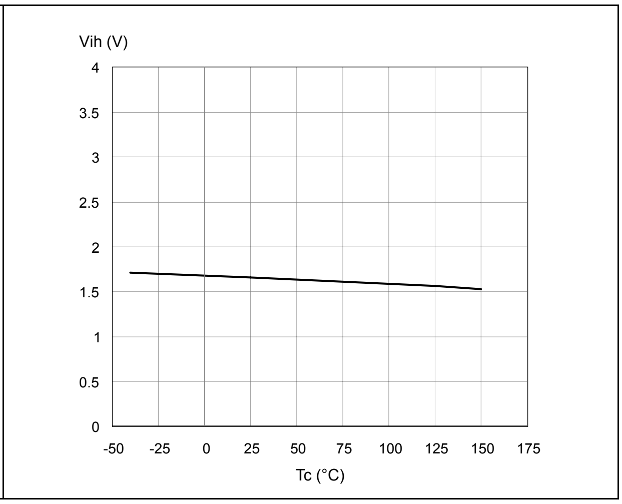


Figure 15. Input low level

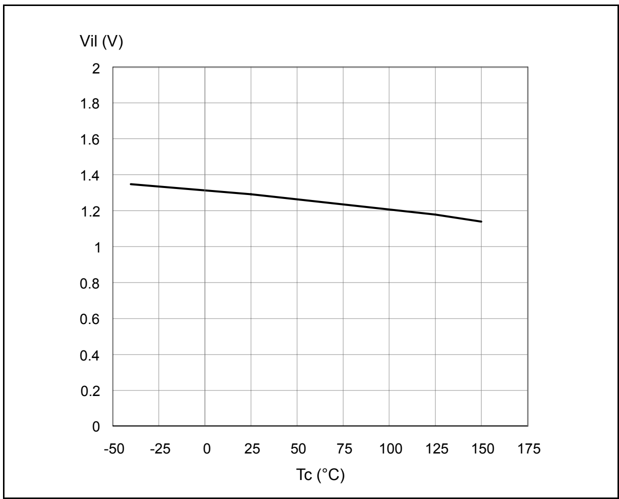


Figure 16. Input hysteresis voltage

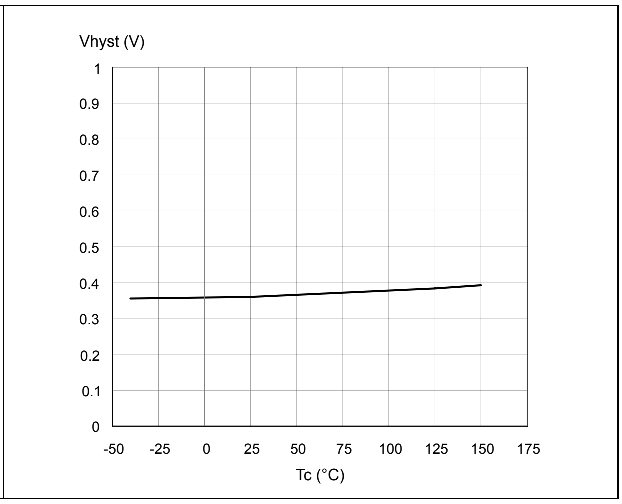


Figure 17. On-state resistance vs T_{case}

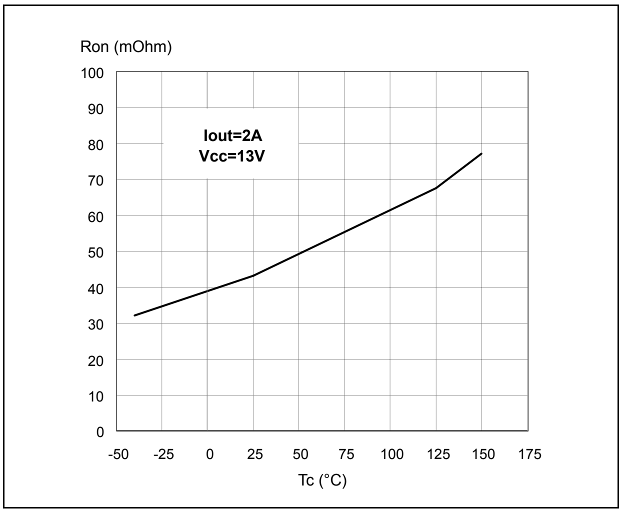


Figure 18. On-state resistance vs V_{CC}

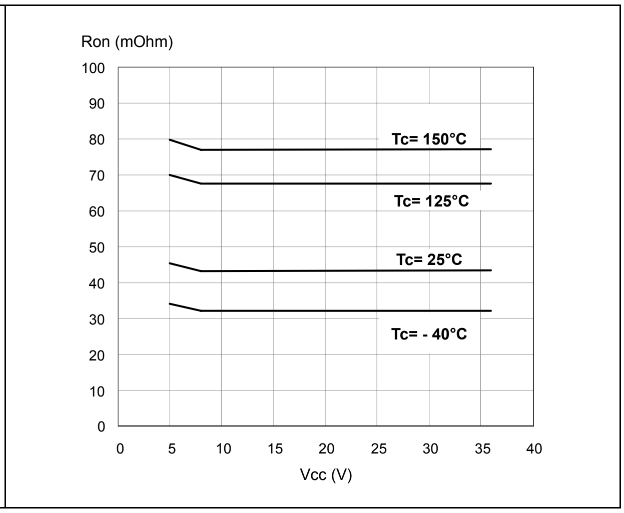


Figure 19. Undervoltage shutdown

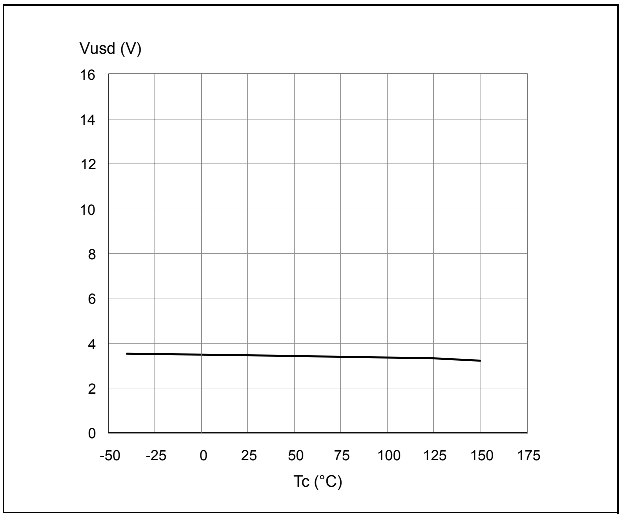


Figure 20. I_{LIMH} vs T_{case}

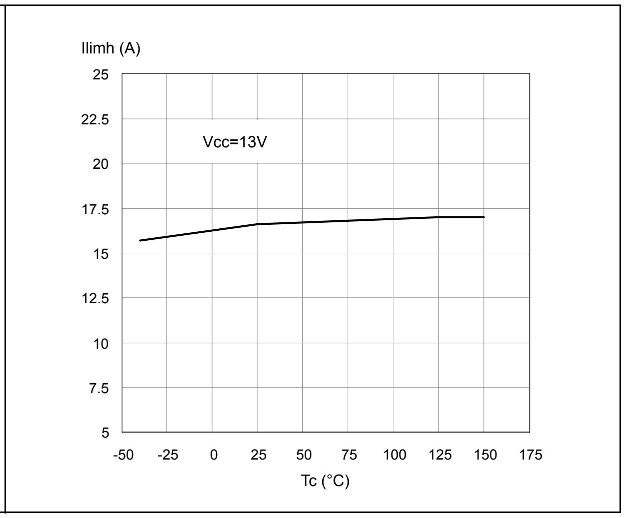


Figure 21. Turn-on voltage slope

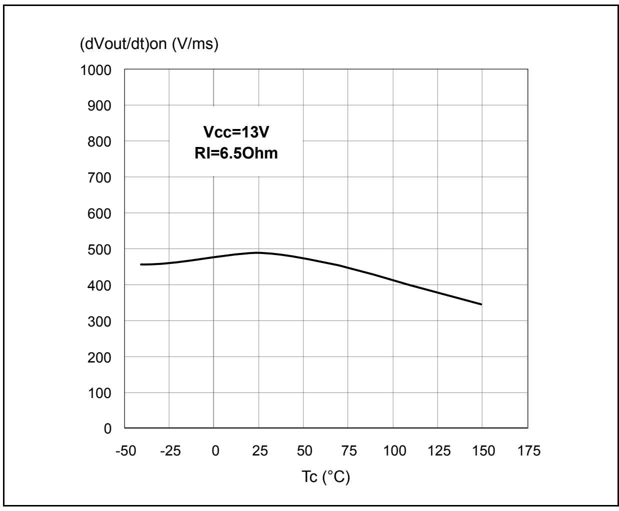


Figure 22. Turn-off voltage slope

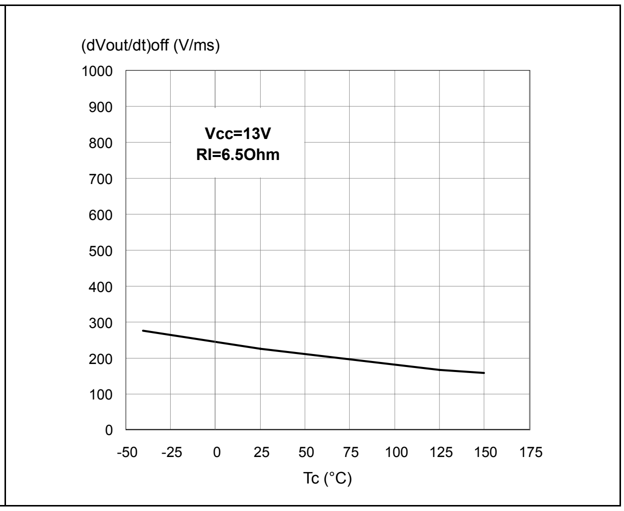


Figure 23. STAT_DIS clamp voltage

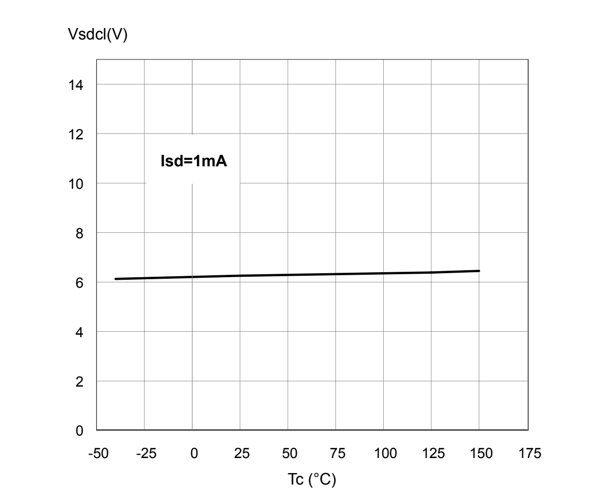


Figure 24. Low level STAT_DIS voltage

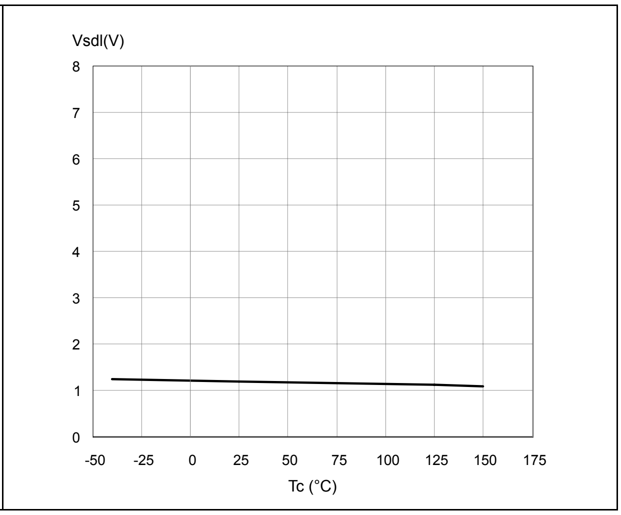
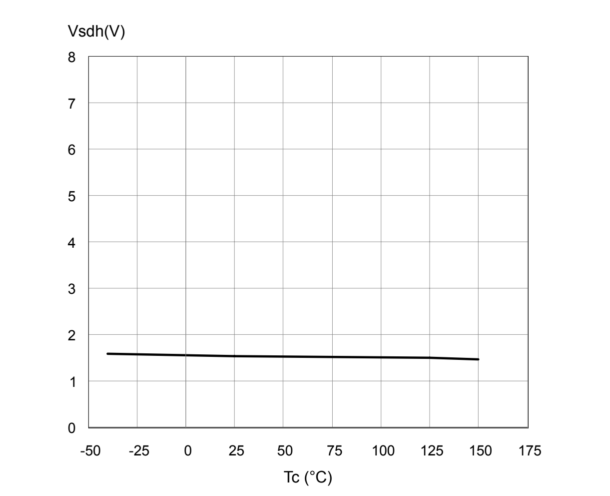
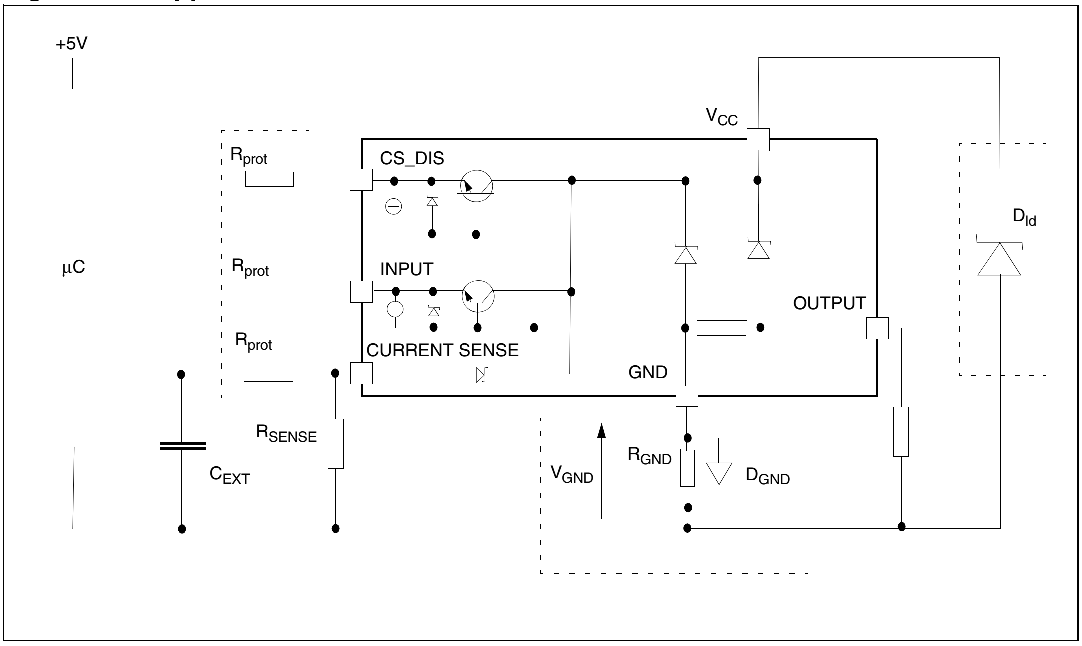


Figure 25. High level STAT_DIS voltage



3 Application information

Figure 26. Application schematic



Note: Channel 2 has the same internal circuit as channel 1.

3.1 GND protection network against reverse battery

3.1.1 Solution 1: resistor in the ground line (R_{GND} only)

This can be used with any type of load.

The following is an indication on how to dimension the R_{GND} resistor.

1. $R_{GND} \leq 600mV / (I_{S(on)max})$.
2. $R_{GND} \geq (-V_{CC}) / (-I_{GND})$

where $-I_{GND}$ is the DC reverse ground pin current and can be found in the absolute maximum rating section of the device datasheet.

Power Dissipation in R_{GND} (when $V_{CC}<0$: during reverse battery situations) is:

$P_D = (-V_{CC})^2/R_{GND}$

This resistor can be shared amongst several different HSDs. Please note that the value of this resistor should be calculated with formula (1) where $I_{S(on)max}$ becomes the sum of the maximum on-state currents of the different devices.

Please note that if the microprocessor ground is not shared by the device ground then the R_{GND} will produce a shift ($I_{S(on)max}$ * R_{GND}) in the input thresholds and the status output values. This shift will vary depending on how many devices are ON in the case of several high side drivers sharing the same R_{GND}.

If the calculated power dissipation leads to a large resistor or several devices have to share the same resistor then ST suggests to utilize Solution 2 (see below).

3.1.2 Solution 2: diode (D_{GND}) in the ground line

A resistor (R_{GND}=1kΩ) should be inserted in parallel to D_{GND} if the device drives an inductive load.

This small signal diode can be safely shared amongst several different HSDs. Also in this case, the presence of the ground network will produce a shift (≈600mV) in the input threshold and in the status output values if the microprocessor ground is not common to the device ground. This shift will not vary if more than one HSD shares the same diode/resistor network.

3.2 Load dump protection

D_{ld} is necessary (Voltage Transient Suppressor) if the load dump peak voltage exceeds the V_{CC} max DC rating. The same applies if the device is subject to transients on the V_{CC} line that are greater than the ones shown in the ISO 7637-2: 2004(E) table.

3.3 Microcontroller I/Os protection

If a ground protection network is used and negative transient are present on the V_{CC} line, the control pins will be pulled negative. ST suggests to insert a resistor (R_{prot}) in line to prevent the µC I/Os pins to latch-up.

The value of these resistors is a compromise between the leakage current of µC and the current required by the HSD I/Os (Input levels compatibility) with the latch-up limit of µC I/Os.

$-V_{CCpeak}/I_{latchup} \leq R_{prot} \leq (V_{OH\mu C}-V_{IH}-V_{GND}) / I_{IHmax}$

Calculation example:

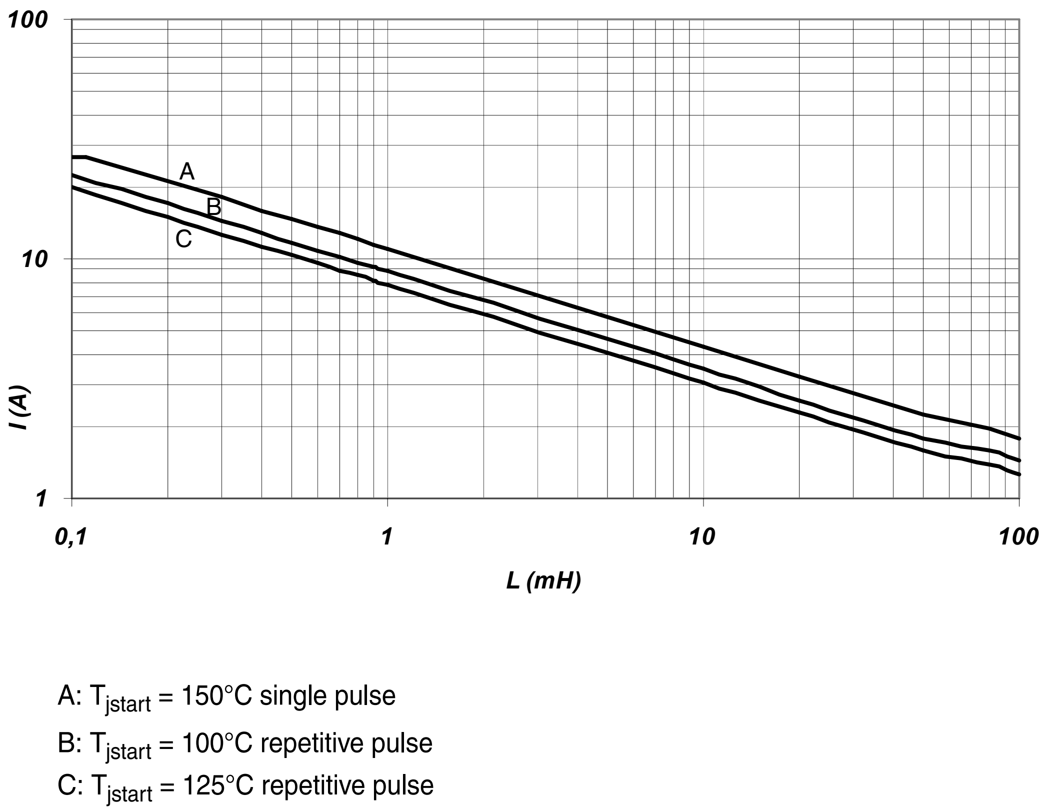
For V_{CCpeak}= - 100V and $I_{latchup} \geq$ 20mA; $V_{OH\mu C} \geq$ 4.5V

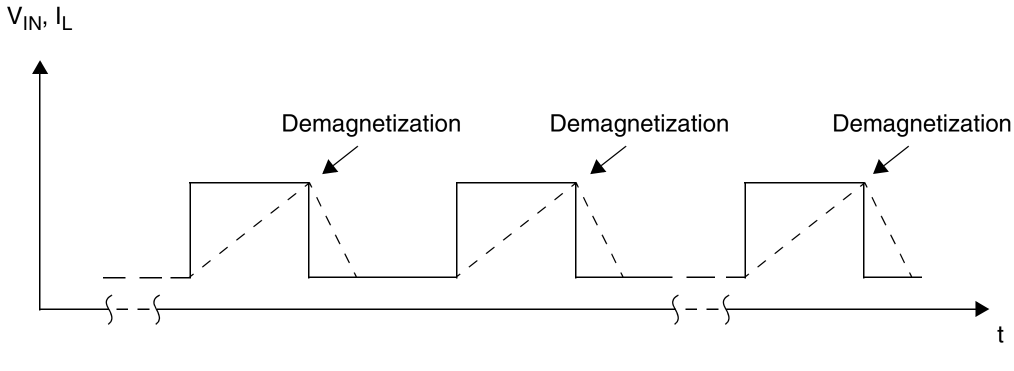
5kΩ ≤ R_{prot} ≤ 180kΩ.

Recommended values: R_{prot} =10kΩ, C_{EXT}=10nF.

3.4 Maximum demagnetization energy (V_{CC} = 13.5V)

Figure 27. Maximum turn-off current versus inductance (for each channel)



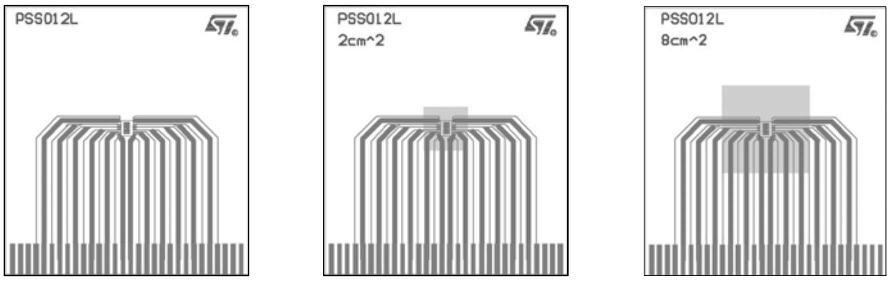


Note: Values are generated with R_L =0 Ω.In case of repetitive pulses, T_{jstart} (at beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves A and B.

4 Package and PCB thermal data

4.1 PowerSSO-12™ thermal data

Figure 28. PowerSSO-12™ PC board



Note: Layout condition of R_{th} and Z_{th} measurements (PCB: Double layer, Thermal Vias, FR4 area= 77 mm x 86 mm,PCB thickness=1.6 mm, Cu thickness=70 µm (front and back side), Copper areas: from minimum pad lay-out to 8 cm^2).

Figure 29. $R_{thj-amb}$ vs PCB copper area in open box free air condition (one channel on)

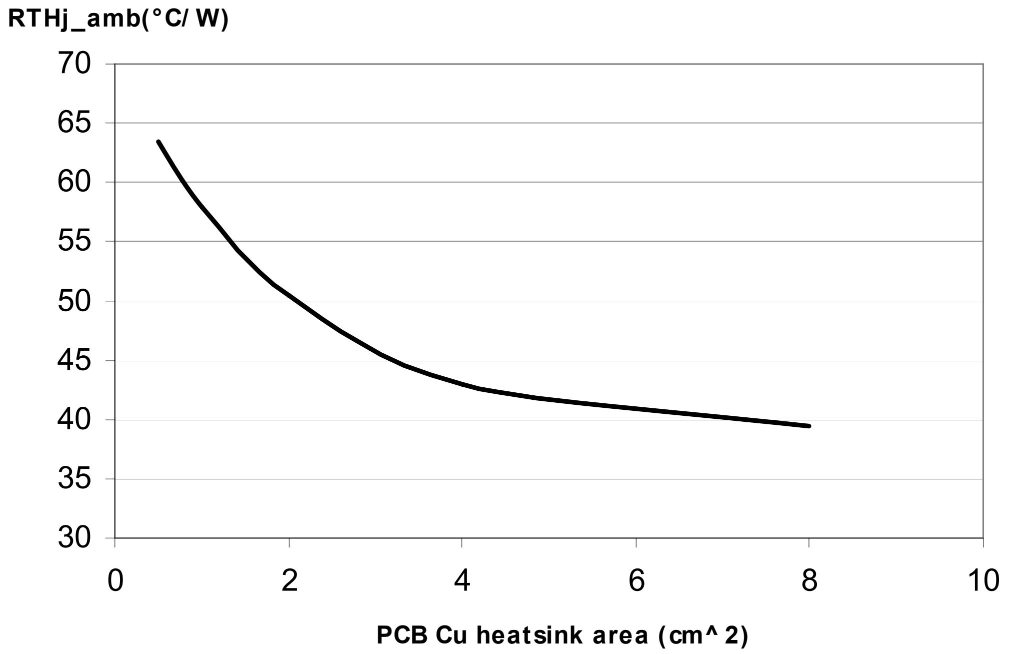
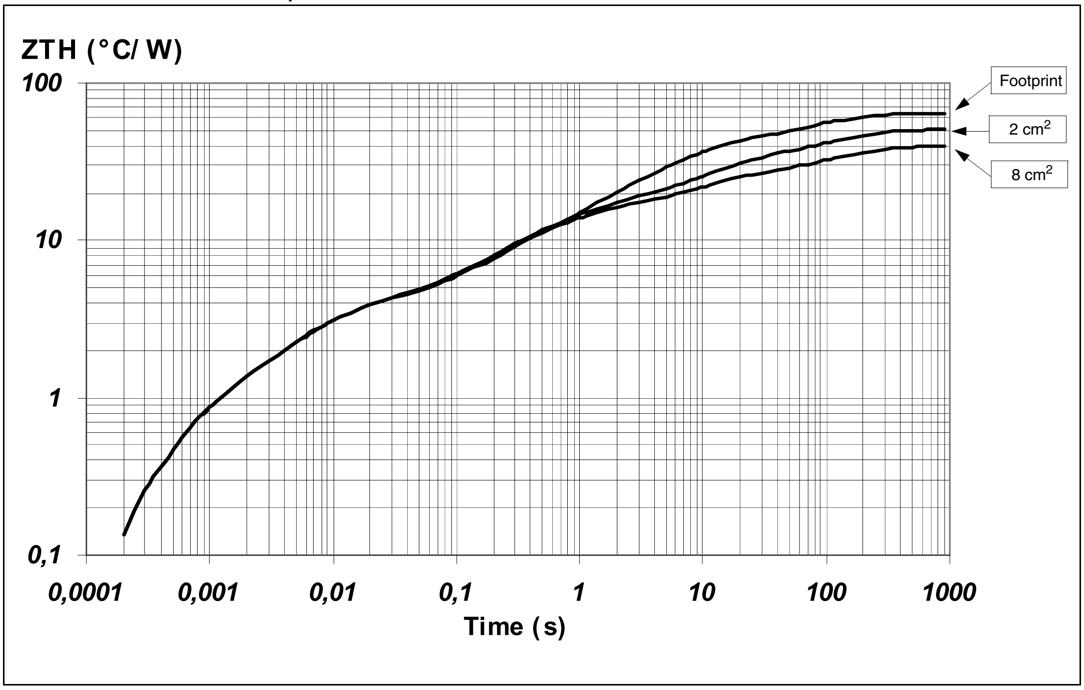


Figure 30. PowerSSO-12™ thermal impedance junction ambient single pulse (one channel on)

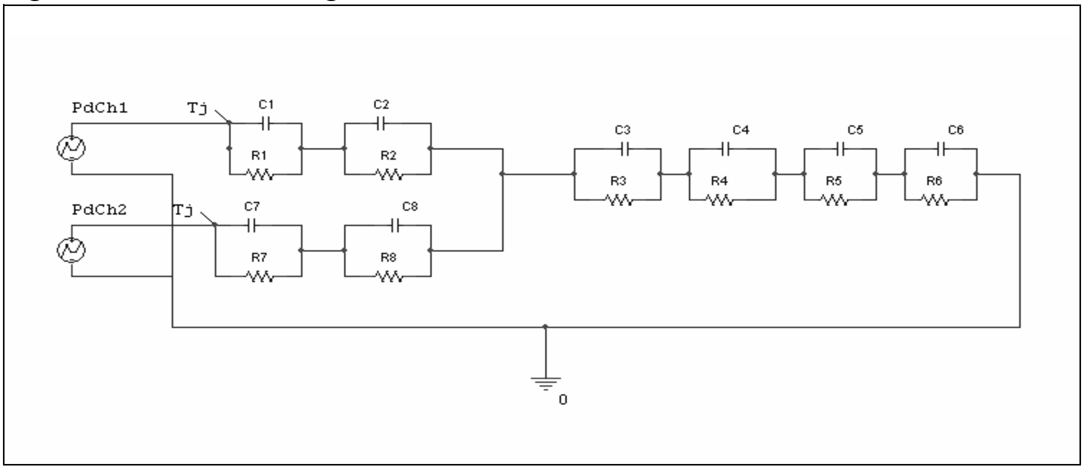


Equation 1: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where $\delta = t_P/T$

Figure 31. Thermal fitting model of a double channel HSD in PowerSSO-12™ [(a)]



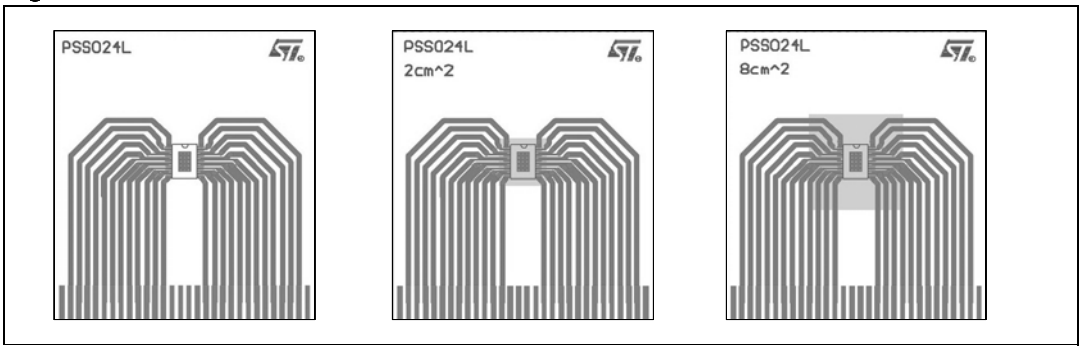
a. The fitting model is a simplified thermal tool and is valid for transient evolutions where the embedded protections (power limitation or thermal cycling during thermal shutdown) are not triggered.

Table 15. PowerSSO-12™ thermal parameter

Area/island (cm^2)	Footprint	2	8
R1= R7 (°C/W)	0.7		
R2= R8 (°C/W)	2.8		
R3 (°C/W)	4		
R4 (°C/W)	8	8	7
R5 (°C/W)	22	15	10
R6 (°C/W)	26	20	15
C1= C7 (W.s/°C)	0.001		
C2= C8 (W.s/°C)	0.0025		
C3 (W.s/°C)	0.05		
C4 (W.s/°C)	0.2	0.1	0.1
C5 (W.s/°C)	0.27	0.8	1
C6 (W.s/°C)	3	6	9

4.2 PowerSSO-24™ thermal data

Figure 32. PowerSSO-24™ PC board



Note: Layout condition of R_{th} and Z_{th} measurements (PCB: Double layer, Thermal Vias, FR4 area= 77 mm x 86 mm, PCB thickness=1.6mm, Cu thickness=70 µm (front and back side), Copper areas: from minimum pad lay-out to 8 cm^2).

Figure 33. $R_{thj\text{-}amb}$ vs PCB copper area in open box free air condition (one channel on)

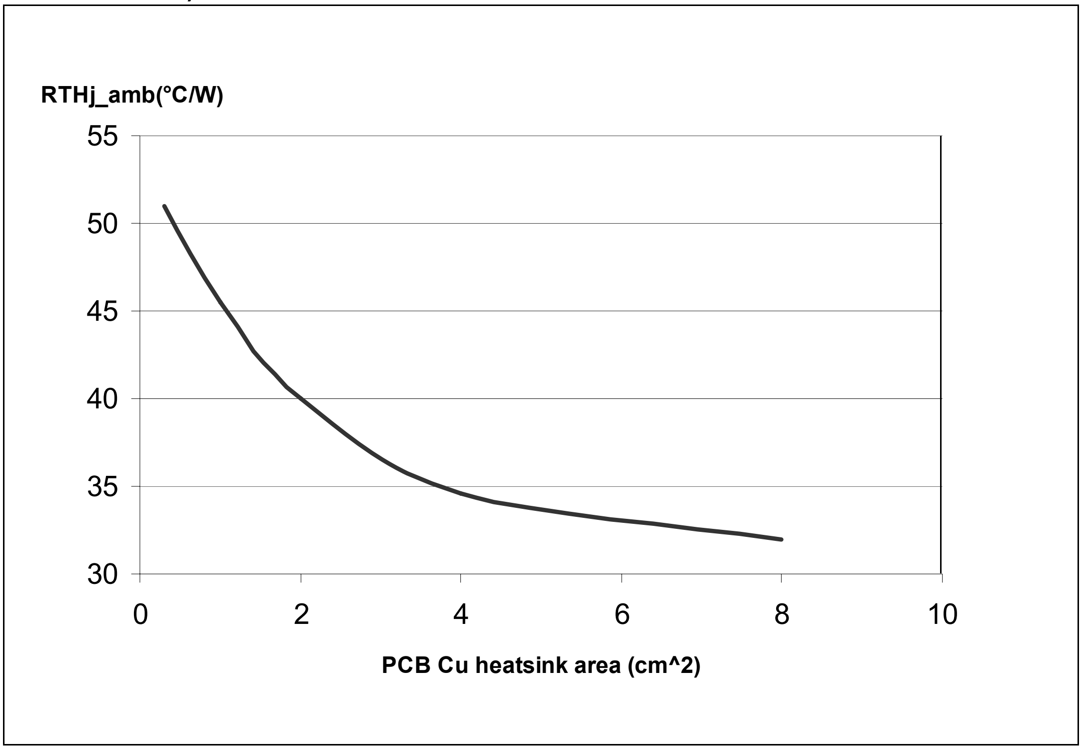
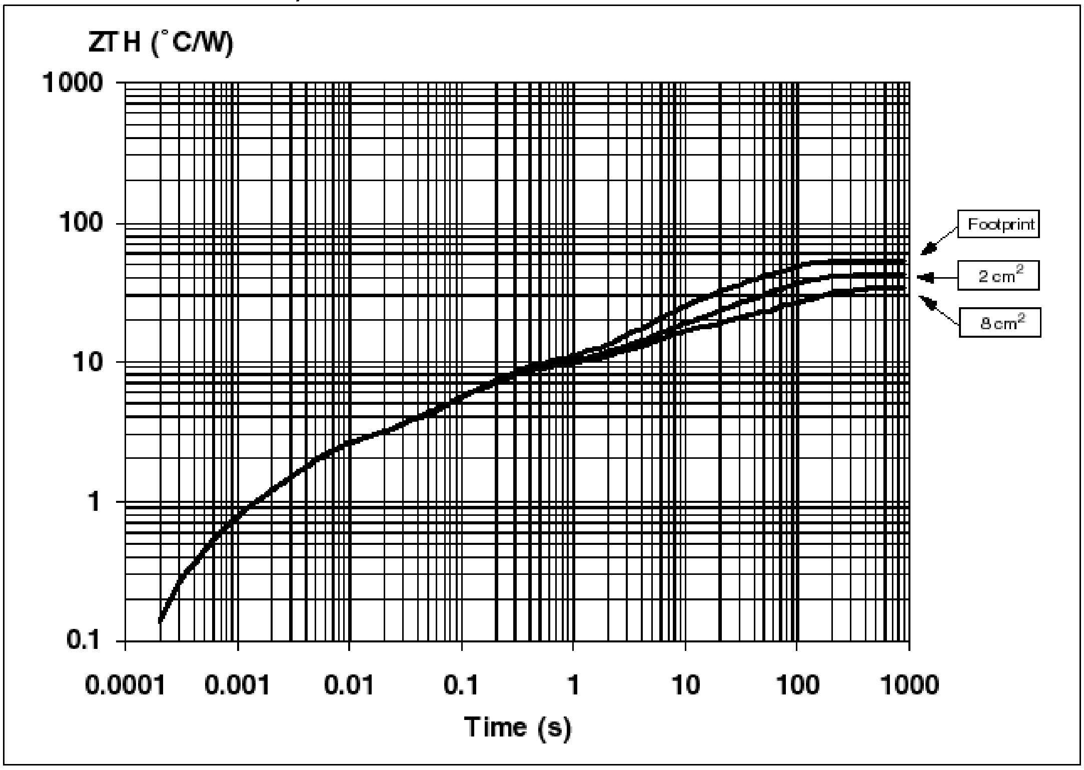


Figure 34. PowerSSO-24™ Thermal impedance junction ambient single pulse (one channel on)

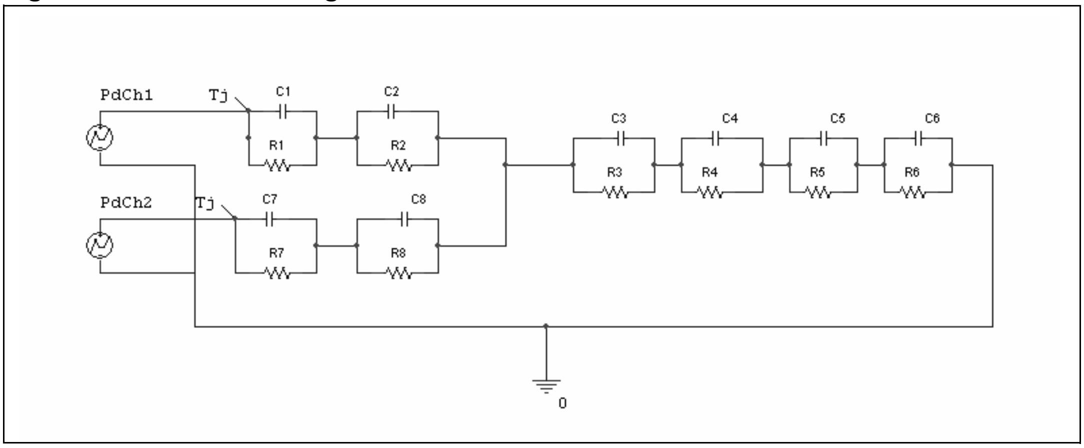


Equation 2: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where $\delta = t_P/T$

Figure 35. Thermal fitting model of a double channel HSD in PowerSSO-24™(b)



b. The fitting model is a simplified thermal tool and is valid for transient evolutions where the embedded protections (power limitation or thermal cycling during thermal shutdown) are not triggered.

Table 16. PowerSSO-24™ thermal parameter

Area/island (cm^2)	Footprint	2	8
R1=R7 (°C/W)	0.4		
R2=R8 (°C/W)	2		
R3 (°C/W)	6		
R4 (°C/W)	7.7		
R5 (°C/W)	9	9	8
R6 (°C/W)	28	17	10
C1=C7 (W.s/°C)	0.001		
C2=C8 (W.s/°C)	0.0022		
C3 (W.s/°C)	0.025		
C4 (W.s/°C)	0.75		
C5 (W.s/°C)	1	4	9
C6 (W.s/°C)	2.2	5	17

5 Package and packing information

5.1 ECOPACK® packages

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com.

ECOPACK® is an ST trademark.

5.2 PowerSSO-12™ package information

Figure 36. PowerSSO-12™ package dimensions

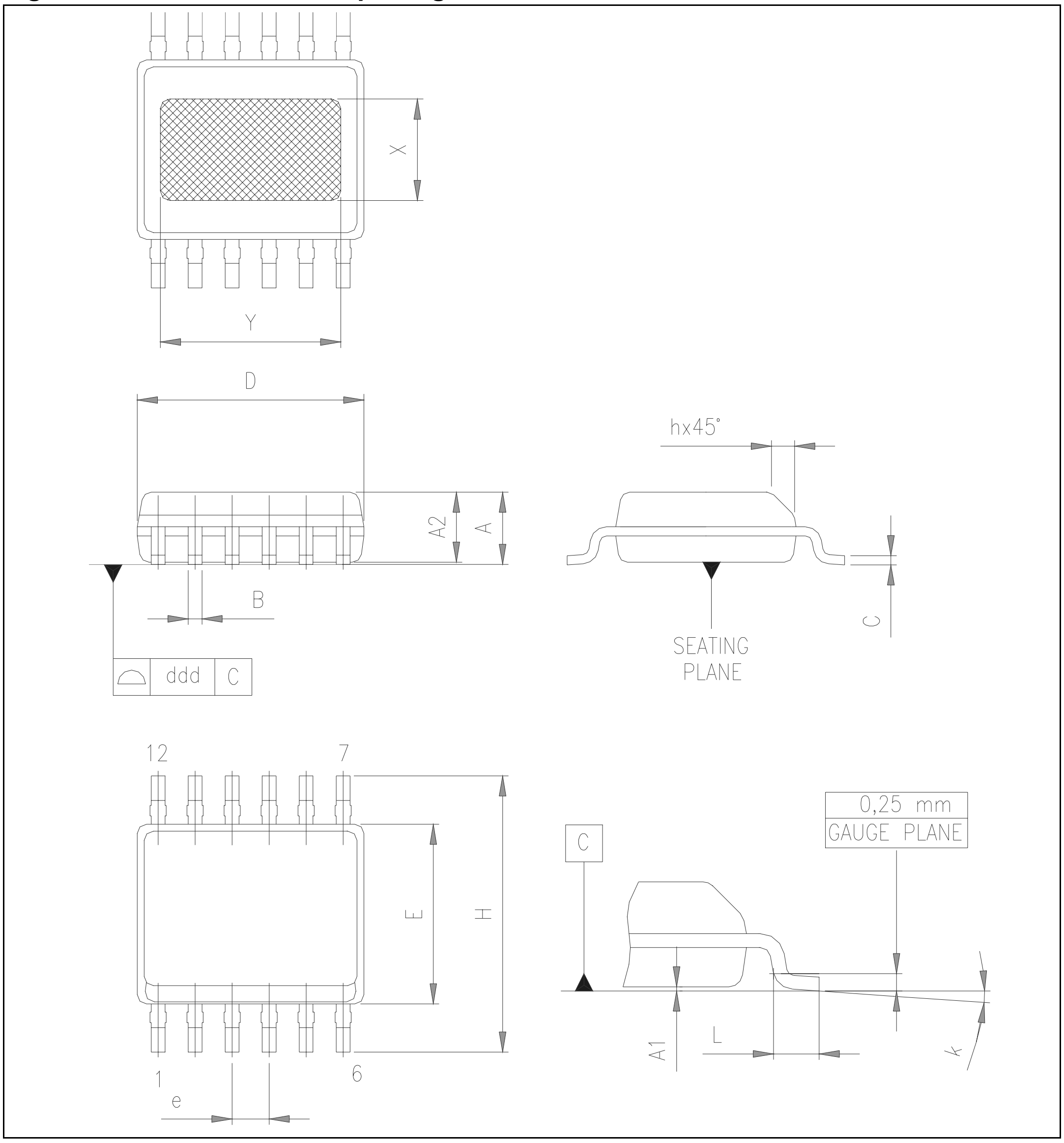


Table 17. PowerSSO-12™ mechanical data

Symbol	Millimeters		
	Min.	Typ.	Max.
A	1.25		1.62
A1	0		0.1
A2	1.10		1.65
B	0.23		0.41
C	0.19		0.25
D	4.8		5.0
E	3.8		4.0
e		0.8	
H	5.8		6.2
h	0.25		0.5
L	0.4		1.27
k	0°		8°
X	1.9		2.5
Y	3.6		4.2
ddd			0.1

5.3 PowerSSO-24™ package information

Figure 37. PowerSSO-24™ package dimensions

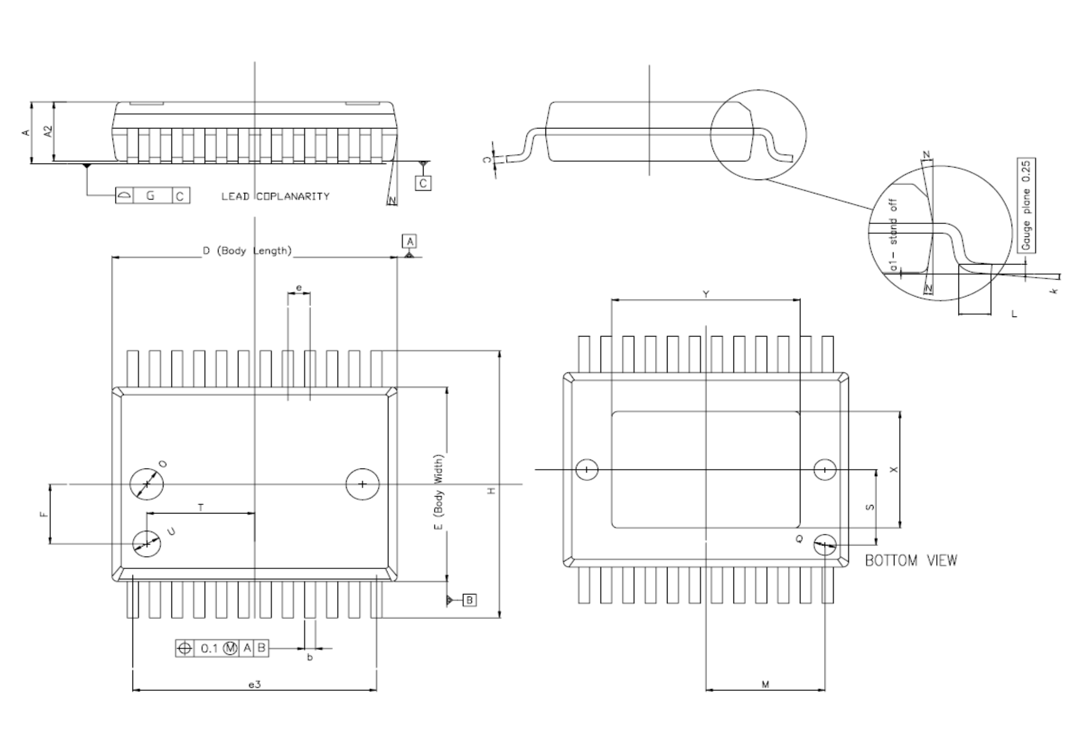


Table 18. PowerSSO-24™ mechanical data

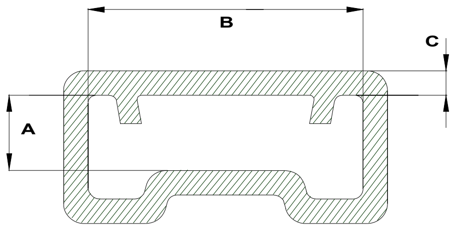
Symbol	Millimeters		
	Min.	Typ.	Max.
A	-		2.45
A2	2.15		2.35
a1	0		0.1
b	0.33		0.51
c	0.23		0.32
D	10.10		10.50
E	7.4		7.6
e		0.8	
e3		8.8	
F		2.3	
G			0.1
H	10.1		10.5

Table 18. PowerSSO-24™ mechanical data (continued)

Symbol	Millimeters		
	Min.	Typ.	Max.
h			0.4
k	0°		8°
L	0.55		0.85
O		1.2	
Q		0.8	
S		2.9	
T		3.65	
U		1.0	
N			10°
X	4.1		4.7
Y	6.5		7.1

5.4 PowerSSO-12™ packing information

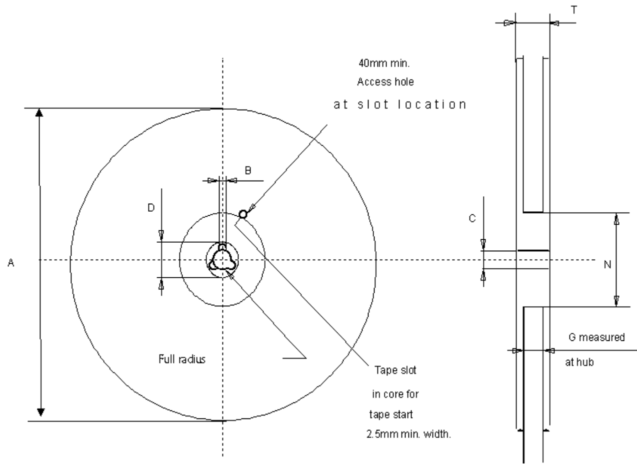
Figure 38. PowerSSO-12™ tube shipment (no suffix)



Base Q.ty	100
Bulk Q.ty	2000
Tube length (± 0.5)	532
A	1.85
B	6.75
C (± 0.1)	0.6

All dimensions are in mm.

Figure 39. PowerSSO-12™ tape and reel shipment (suffix “TR”)



REEL DIMENSIONS

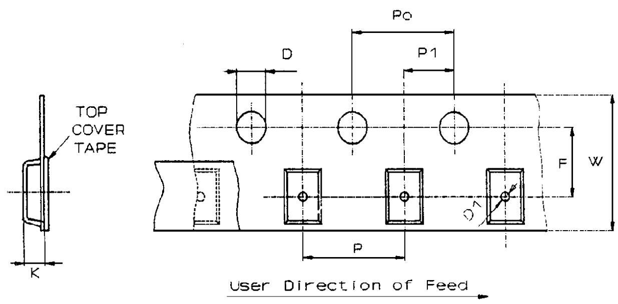
Base Q.ty	2500
Bulk Q.ty	2500
A (max)	330
B (min)	1.5
C (± 0.2)	13
F	20.2
G (+ 2 / -0)	12.4
N (min)	60
T (max)	18.4

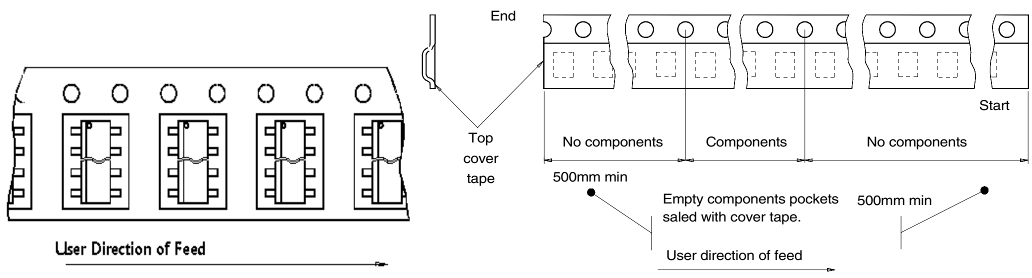
TAPE DIMENSIONS

According to Electronic Industries Association (EIA) Standard 481 rev. A, Feb. 1986

Tape width	W	12
Tape Hole Spacing	P0 (± 0.1)	4
Component Spacing	P	8
Hole Diameter	D (± 0.05)	1.5
Hole Diameter	D1 (min)	1.5
Hole Position	F (± 0.1)	5.5
Compartment Depth	K (max)	4.5
Hole Spacing	P1 (± 0.1)	2

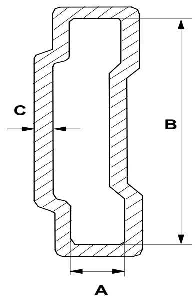
All dimensions are in mm.





5.5 PowerSSO-24™ packing information

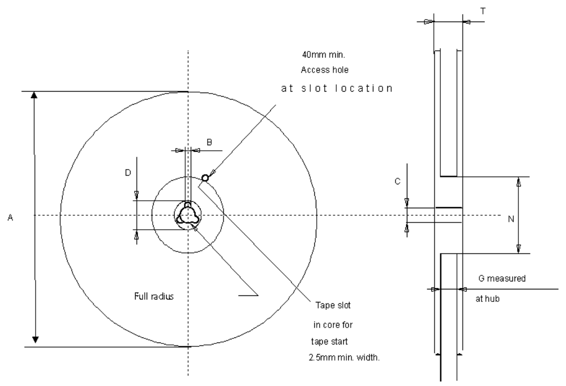
Figure 40. PowerSS0-24™ tube shipment (no suffix)



Base Qty	49
Bulk Qty	1225
Tube length (±0.5)	532
A	3.5
B	13.8
C (±0.1)	0.6

All dimensions are in mm.

Figure 41. PowerSSO-24™ tape and reel shipment (suffix "TR")



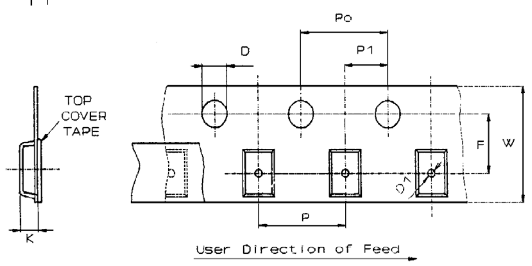
REEL DIMENSIONS

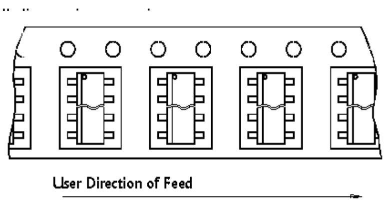
Base Qty	1000
Bulk Qty	1000
A (max)	330
B (min)	1.5
C (± 0.2)	13
F	20.2
G (+2 / -0)	24.4
N (min)	100
T (max)	30.4

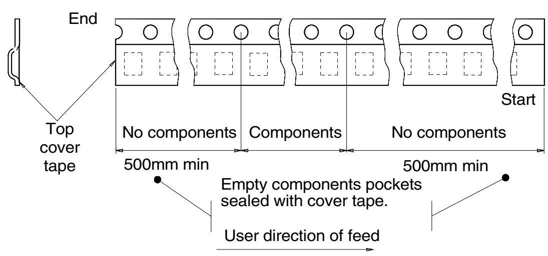
TAPE DIMENSIONS

According to Electronic Industries Association (EIA) Standard 481 rev. A, Feb. 1986

Tape width	**W**	24
Tape Hole Spacing	**P0 (± 0.1)**	4
Component Spacing	**P**	12
Hole Diameter	**D (± 0.05)**	1.55
Hole Diameter	**D1 (min)**	1.5
Hole Position	**F (± 0.1)**	11.5
Compartment Depth	**K (max)**	2.85
Hole Spacing	**P1 (± 0.1)**	2







6 Revision history

Table 19. Document revision history

Date	Revision	Changes
30-Mar-2006	1	Initial release.
14-Apr-2006	2	PowerSSO-24 dimensions table update.
26-Apr-2007	3	Reformatted *Figure 31* title corrected
14-May-2007	4	*Table 4*: corrected E_{MAX} value. *Table 10*: added dk1/k1, dk2/k2, dk3/k3, $\Delta t_{DSENSE2H}$. Added *Figure 5*. Updated *Figure 6*. Added *Figure 7*. *Table 12*: Updated test level values III and IV for test pulse 5b and notes. Added *Section 3.4: Maximum demagnetization energy (VCC = 13.5V)*.
01-Jun-2007	5	*Figure 31: Thermal fitting model of a double channel HSD in PowerSSO-12™*, *Figure 35: Thermal fitting model of a double channel HSD in PowerSSO-24™*: added notes.
04-Dec-2007	6	Updated *Table 10: Current sense (8V<V_{CC}<16V)*: – changed $t_{DSENSE2H}$ max value from 300 µs to 250µs. – added I_{OL} parameter. Updated *Section 4.1: PowerSSO-12™ thermal data*: – Changed *Figure 29: Rthj-amb vs PCB copper area in open box free air condition (one channel on)*. – Changed *Figure 30: PowerSSO-12™ thermal impedance junction ambient single pulse (one channel on)*. – Updated *Table : *: R3 value changed from 7 to 4 °C/W. R4 values changed from 10 /10 /10 to 8 /8 /7 °C/W.
12-Feb-2008	7	Corrected typing error in *Table 10: Current sense (8V<V_{CC}<16V)*: changed I_{OL} test condition from V_{IN} = 0V to V_{IN} = 5V.
16-Jun-2009	8	*Table 18: PowerSSO-24™ mechanical data*: – Deleted A (min) value – Changed A (max) value from 2.47 to 2.45 – Changed A2 (max) value from 2.40 to 2.35 – Changed a1 (max) value from 0.075 to 0.1 – Added F and k rows
21-Jul-2009	9	Updated *Figure 37: PowerSSO-24™ package dimensions*. Updated *Table 18: PowerSSO-24™ mechanical data*: – Deleted G1 row – Added O, Q, S, T, and U rows